

A1 15, a 16-bit timer/counter 17, multipurpose inputs/outputs 19 and a crystal oscillator/buffer 21.--

IN THE CLAIMS:

Please amend claims 3, 4, and 7-9 as follows:

A2 3. (Amended) The UART of claim 1 wherein said programmable register comprises a shadow register which is a write-only register with the same address as a read-only register only read by a user.

4. (Amended) The UART of claim 3 wherein said write-only register comprises the first 4 bits of a modem status register.

A3 7. (Amended) A universal asynchronous receiver transmitter (UART) comprising:
a first-in, first-out (FIFO) buffer;
a circuit for detecting a last word transmitted from said FIFO buffer;
a transmitter empty circuit for generating a transmitter empty signal on a transmitter empty control line when a last word transmitted from said FIFO buffer is detected, wherein said transmitter empty signal is an internal signal triggered from a stop bit of said last word;
a delay circuit for delaying generation of said transmitter empty signal for a programmable delay time;
a programmable register for setting said programmable delay time, wherein said programmable register comprises a shadow register which is a write-only register with the same address as a read-only register only read by a user;
a plurality of channels, each channel having said FIFO buffer, said circuit for detecting a last word and said transmitter empty circuit; and